VOLTAGE RAMP GENERATOR AND CURRENT RAMP GENERATOR INCLUDING SUCH A GENERATOR

Field of the Invention

The present invention relates to a voltage ramp generator, and to a current ramp generator that converts the voltage ramp generator into the current ramp generator. The present invention has a particularly advantageous application for DC voltage converters operating in a current mode, for example.

Background of the Invention

Circuits for DC voltage converters operating in a current mode include a regulation circuit that includes a current ramp generator necessary to stabilize the regulation circuit. It is therefore necessary for the current ramp generator to have only slight component and temperature variations.

A current ramp generator in accordance with the prior art is shown in Figure 1. The current ramp generator is made up of a voltage ramp generator circuit and a circuit that enables the voltage ramp to be converted into a current ramp. The voltage ramp generator circuit is made up of a current generator Ig1 and a capacitance C. The current Ig1 charges the capacitance C in accordance with the equation:

$$\frac{\Delta Vc}{\Delta t} = \frac{1}{C} \times Ig1$$

where Vc is the voltage at the terminals of the capacitance C.

As is known to those skilled in the art, the current Ig1 can be written as:

$$Ig1 = K1 \times \frac{Vg1}{Rg1}$$

where Vg1 is a reference voltage such as a Bandgap voltage, for example, and Rg1 is the resistance of the current generator, and K1 is a proportionality coefficient.

The circuit permits the conversion of the voltage ramp into a current ramp, and is made up of an operational amplifier A, three transistors T1, T2, T3 and a resistance Rs. The operational amplifier A includes a first input (e-), a second input (e+) and an output. The transistor T1 is a N-type MOS transistor including a gate, a source and a drain, and the transistors T2 and T3 are P-type MOS transistors, each including a gate, a source and a drain.

The first input (e-) of the operational amplifier A is connected to the source of the transistor T1. The gate of which is connected to the output of the operational amplifier A, and the drain is connected to the drain of transistor T2. The second input (e+) of the operational amplifier A is connected to the first terminal of the capacitance C. The second terminal the capacitance C is connected to ground. The source of transistor T1 is connected to the first terminal of the resistance Rs, and the second terminal of which is connected to ground.

The transistors T2 and T3 are assembled as a current mirror. The source of transistor T2 is connected to a supply voltage V+. The drain and the gate of transistor T2 are connected to one another and to the gate of transistor T3. The source of transistor T3 is connected to the supply voltage V+, and the drain

is connected to the circuit (not shown in the figure) which collects the current Is. Variation of the current Is is in relation to time which forms the current ramp.

In a known way, the variation of the current Is in relation to time is given by the equation:

$$\frac{\Delta Is}{\Delta t} = \frac{1}{C} \times \frac{Vg1}{Rg1} \times K1 \times \frac{1}{Rs}$$

It follows that the variation of the gradient $\frac{\Delta Is}{\Delta t}$ depends directly on the variations of resistances Rg1 and Rs and of the capacitance C. The resistances Rg1 and Rs can have a spread on the order of ± 20%. These spreads are then reflected in the current ramp on the order of ± 40%.

Prior approaches for correcting the current ramp spreads include adjusting the resistance Rs. It is then necessary to use a sequence of tests to adjust the value of resistance Rs. Provision is thus made to use fuse type memory points to adjust the ramp of each circuit. This adjustment is a tedious operation. Furthermore, the design of the resistance Rs produced as a combination of fuses requires a relatively large area of the circuit.

In addition, resistances Rg1 and Rs have temperature variations. These variations also have an impact on the current ramp. Since the adjustment of resistance Rs is only valid at the temperature at which it is carried out, the temperature dependence is not corrected.

Background of the Invention

In view of the foregoing background, the present invention does not have the above described disadvantages. In effect, the invention relates to a voltage ramp generator comprising a capacitance and a charging circuit that permits the generation of a charging current for the capacitance. The charging circuit for the capacitance comprises a current generator of resistance Rg2. The charging circuit for the capacitance includes means that permit the charging current for the capacitance to be proportional to $(Re/Rg2)^2$, where Re is a resistance.

According to one particularly advantageous embodiment of the invention, the means that permit the charging current for the capacitance to be proportional to the quantity $(Re/Rg2)^2$ comprises a degenerate current mirror. The term degenerate current mirror is used to mean a current mirror whose current ratio is not equal to the ratio of the surface areas of the MOS transistors that makes it up.

The invention also relates to a current ramp generator comprising a voltage ramp generator and a circuit that permits the conversion of the voltage ramp to a current ramp. The voltage ramp generator is a voltage ramp generator such as the one mentioned above.

According to the preferred embodiment of the invention, the components forming the voltage ramp generator and the current ramp generator are produced using CMOS technology. The invention also relates to where the components are produced using a different technology, such as bipolar technology, for example.

Brief Description of the Drawings

Other characteristics and advantages of the invention will become apparent on reading a description of a preferred embodiment of the invention made making reference to the appended figures among which:

Figure 1 shows a current ramp generator according to the prior art,

Figure 2 shows a voltage ramp generator according to the preferred embodiment of the present invention, and

Figure 3 shows a current ramp generator according to the preferred embodiment of the present invention.

Detailed Description of the Preferred Embodiments

In all the figures, the same reference numbers designate the same components. Figure 2 represents a voltage ramp generator according to the preferred embodiment of the present invention. The voltage ramp generator circuit includes a current generator Ig2, a resistance Re, a capacitance C and two P-type MOS transistors T4 and T5 each comprising a gate, a drain and a source.

The transistor T4 has its source connected to a first terminal of the resistance Re, the second terminal of which is connected to a supply voltage V+. The drain and the gate of transistor T4 are connected to a first terminal of the current generator Ig2, the second terminal of which is connected to ground. The transistor T5 has its gate connected to the gate of transistor T4, its source connected to the supply voltage V+ and its drain connected to a first terminal of the capacitance C. The second terminal of the capacitance C is connected to ground.

Preferably, the substrate effect is suppressed on transistors T4 and T5, and the voltage threshold Vth4 of transistor T4 is equal to the voltage threshold Vth5 of transistor T5. Current Ig2 passes through the resistance Re. Therefore, it follows that:

$$Re \times Ig2 + VGST4 - Vth4 = VGST5 - Vth5,$$

where VGST4 is the gate/source voltage of transistor T4 and VGST5 is the gate/source voltage of transistor T5.

According to the invention, the resistance Re is chosen in such a way that:

Re x Ig2 >> VGST4 - Vth4,

It follows therefore:

VGST5 - Vth5 ≠ Re x Ig2,

In CMOS technology, the current which passes through the transistor T5 is written as:

$$I_{T5} = \frac{\mu \times Cox}{2} \times \frac{W}{L} \times \left(V_{GST5} - Vth5\right)^2 ,$$

where μ is the mobility of the carriers, Cox is the gate capacitance of the transistor T5, W is the channel width of transistor T5, L is the channel length of transistor T5.

It follows, therefore, that:

$$I_{T5} = \frac{\mu \times Cox}{2} \times \frac{W}{L} \times \left(\mathrm{Re} \times Ig2\right)^2 ,$$

The current Ig2 can be written as:

$$Ig2 = K2 \times \frac{Vg2}{Rg2} ,$$

where Vg2 is a reference voltage, Rg2 is the resistance of the current generator and K2 is a proportionality coefficient.

Preferably, the voltage Vg2 is proportional to the quantity $k\frac{T}{q}$, where k is the Boltzmann constant, T is absolute temperature and q is the charge of an electron.

It follows, therefore, that:

$$I_{T5} = \frac{\mu \times Cox}{2} \times \frac{W}{L} \times \left(\frac{\mathrm{Re}}{Rg2} \right)^2 \times K2^2 \times Vg2^2 .$$

The current IT5 is the current which charges the capacitance C. The equation which translates the charge of the capacitance C is written as:

$$\frac{\Delta Vc}{\Delta t} = \frac{1}{C} \times \frac{\mu \times Cos}{2} \times \frac{W}{L} \times \left(\frac{\mathrm{Re}}{Rg2} \right)^2 \times K2^2 \times Vg2^2 .$$

The presence of the resistance Re advantageously permits compensation for the variations of the resistance Rg2. The resistances Re and Rg2 are chosen to be of the same type of technology, thereby allowing compensation for their spreads.

It is then possible, for example, to obtain a variation of the gradient $\frac{\Delta Vc}{\Delta t}$ on the order of ± 25% for a variation of resistances Rg2 and Re, each on the order of ± 40% in total. The resistance Re is preferably chosen with a temperature variation coefficient of the same order of magnitude as that for the resistance Rg2. It is then possible to compensate for variations in temperature due to the resistance Rg2. Preferably, as has been previously mentioned, the voltage Vg2 is proportional to the quantity $k\frac{T}{q}$. The

mobility of the carriers varies proportionately to $T^{-3/2}$.

It follows that the voltage ramp $\frac{\Delta Vc}{\Delta t}$ varies proportionately to $T^{1/2}$.

Figure 3 shows a current ramp generator according to the preferred embodiment of the invention. The current ramp generator includes a voltage ramp generator circuit such as that described in Figure 2, and a circuit that allows the voltage ramp to be converted into a current ramp.

The circuit allowing the conversion of the voltage ramp into a current ramp is made up of operational amplifier A, three transistors T1, T2, T3 and a resistance Rs. The three transistors T1, T2, T3 and the resistance Rs are connected as shown in Figure 1. Similarly, the first input (e-) of the operational amplifier A is connected to the source of transistor T1, the gate of which is connected to the output of the operational amplifier. The second input (e+) of the operational amplifier A is connected to a first terminal of the capacitance C. The second terminal of the capacitance C is connected to ground.

Since Is is the current passing through transistor T3, the current ramp $\frac{\Delta Is}{\Delta t}$ is written as:

$$\frac{\Delta Is}{\Delta t} = \frac{1}{Rs} \times \frac{\Delta Vc}{\Delta t},$$

where $\frac{\Delta Vc}{\Delta t}$ is the voltage ramp such as that calculated in the description of Figure 2. Hence, all the advantages described for the voltage ramp generator circuit in Figure 2 are also advantages that relate to the current ramp generator according to the invention.

As has already been previously mentioned, the voltage ramp $\frac{\Delta Vc}{\Delta t}$ varies with temperature according to $T^{1/2}$.

In accordance with the preferred embodiment of the invention, the resistance Rs is an implanted N-type resistance with a positive temperature variation coefficient that enables the temperature variation of the current ramp to vary according to T^n, where n is less than $\frac{1}{2}$. To reduce the effect of component variations on the ramp, the capacitance C is the gate capacitance of a MOS transistor, the spread of which compensates for the spread of transistor T5.